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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,659	09/25/2003	Ho Dai Truong	SP047.C9	5208

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EXAMINER	
LAM, TUAN THIEU	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,659	TRUONG ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/2/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 8/2/2004. Claims 20-29 are under examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 20-29 remain rejected under 35 U.S.C. 102(b) as being anticipated by Walters, Jr (USP 5,041,738), prior art of record. Figure 1 shows a clock generator comprising input clock portion (12), first and second output clock signals (Φ1 and Φ2), first feedback path (24), second feedback path (26) for coupling said first and second output clock signals to the input portion, determining if first and second clock signals generated by said first and second clock outputs, respectively, have clock edges that are non-overlapping for a predetermined time T (figures 2a-2c), adding/removing one or more delay elements (figures 4b and 4d shows each delay element N2 and N6 comprises a plurality of delay elements) to said firs and second feedback paths if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T as called for in claims 20 and 25.

Regarding claims 21 and 26, adding a delay element to one of said first or second feedback paths comprises opening a first switch and closing a second switch along said first and second feedback (as shown in figures 4b and 4d shows each delay element N2 and N6 comprises a plurality of delay elements and switches (fuses)).

Regarding claims 22-24 and 27-29, the limitations are anticipated by the fuses used in figure 4.

3. Claims 20-21 and 25-26 remain rejected under 35 U.S.C. 102(b) as being anticipated by Japanese patent (JP 2-124627), prior art cited in the PTOL-1449. Figure 1 shows a clock generator comprising input clock portion (1), first and second output clock signals (2 and 3), first feedback path (5), second feedback path (8) for coupling said first and second output clock signals to the input portion, determining if first and second clock signals generated by said first and second clock outputs, respectively, have clock edges that are non-overlapping for a predetermined time T (figure 2), adding/removing one or more delay elements (figure 3 shows each delay element 5 and 8 in the feedback paths comprises a plurality of delay elements 13-15) to said first and second feedback paths if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T as called for in claims 20 and 25.

Regarding claims 21 and 26, adding a delay element to one of said first or second feedback paths comprises opening a first switch and closing a second switch along said first and second feedback (as shown in figures 3 shows each delay element 5 and 8 comprises a plurality of delay elements and switches (16, 17)).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 22-24 and 27-29 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese patent JP 2-124627 in view of Walters, Jr. (USP 5,041,738), both prior art cited in the PTOL-1449. Figure 1 of JP 2-124627 shows a clock generator comprising input clock portion (1), first and second output clock signals (2 and 3), first feedback path (5), second feedback path (8) for coupling said first and second output clock signals to the input portion, determining if first and second clock signals generated by said first and second clock outputs, respectively, have clock edges that are non-overlapping for a predetermined time T (figure 2), adding/removing one or more delay elements (figure 3 shows each delay element 5 and 8 in the feedback paths comprises a plurality of delay elements 13-15) to said first and second feedback paths if said first and second clock signals do not have clock edges that are non-overlapping for said predetermined time T.

The difference between JP 2-124627 and the present invention is that the JP reference uses electrical switches (16, 17), i.e., transistors instead of fuses as called for in claims 22-24 and 27-29. Walters, Jr. uses fuses for controlling non-overlapping time instead of using transistors switches. Using fuses is cheaper and allow the non-overlapping time be adjusted after fabrication. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace JP 2-124627's transistor switches with fuses because fuses are cheap and it would allow the non-overlapping time be adjusted after fabrication.

Response to Arguments

6. Applicant's arguments filed 8/2/2004 have been fully considered but they are not persuasive.

Regarding the rejection of claims 20-29 under 35USC as being anticipated by Walters, Jr.

(USP 5,041,738), applicant argues that Walters Jr. does not teach an apparatus that includes..a first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion as called for in claim 20. Rather, Walters Jr. shows lines 24 and 26 couple a clock output to **an internal node within the phase generating circuits** 22 and 18, respectively, is not persuasive. As shown in figure 1, the output clock is being input to the input portion via the drain/source of the pass gate N6/N2 transistor. Therefore, the output clock signal is coupled to the node via the input transistor N6/N2. Therefore, the limitation of first feedback path for coupling said first clock output to said clock input portion, and a second feedback path for coupling said second clock output to said clock input portion are fully met.

Applicant further argues that Walters Jr. does not teach adding one or more delay elements to said first and/or second feedback paths is not persuasive. As seen from figure 1 of Walters Jr., the delay elements are the transistors N2/N6 and the fuses F4/F2. The plurality of those delay elements are further illustrated in figures 4A-4d. The combination of transistors and fuse receive the output clock and pass the output clock signal to the nodes A or B. The impedance of the transistor and the fuse determines how much the output signal be delayed, thus, the amount of overlapping. Therefore, the limitation of adding one or more delay elements to said first and/or second feedback paths is fully met.

Regarding the rejection of claims 20 and 25 as being anticipated by JP 2-124627, applicant argues that the present invention calls for adding one or more delay elements or removing one or delay elements from feedback paths of an apparatus during manufacturing is distinct from JP 2-124627 is not persuasive. The limitation of "**during manufacturing**" is not

in the claims 20 25. Further, as stated in the rejection under 35USC 103(a) as being unpatentable over JP 2-124627 in view of Walters Jr., one skilled in the art would have recognize the advantages of using fuses over transistors. Using fuses is cheaper and allow the non-overlapping time be adjusted during and after fabrication. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to replace JP 2-124627's transistor switches with fuses because fuses are cheap and it would allow the non-overlapping time be adjusted after fabrication. Therefore, claims 20-29 remain rejected.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

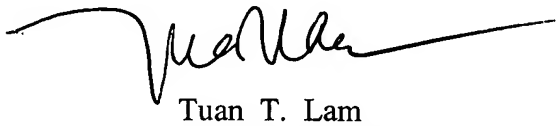
Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant's cited prior art has been carefully considered.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan T. Lam
Primary Examiner
Art Unit 2816

9/16/2004